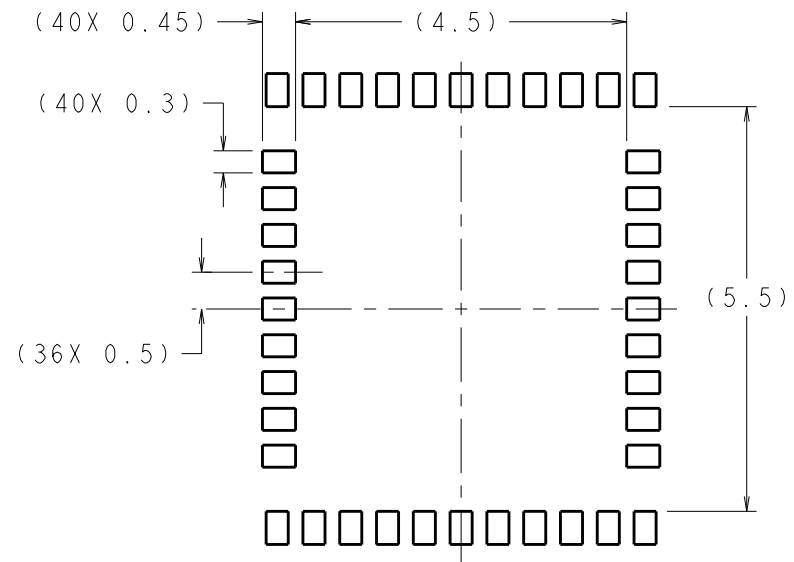
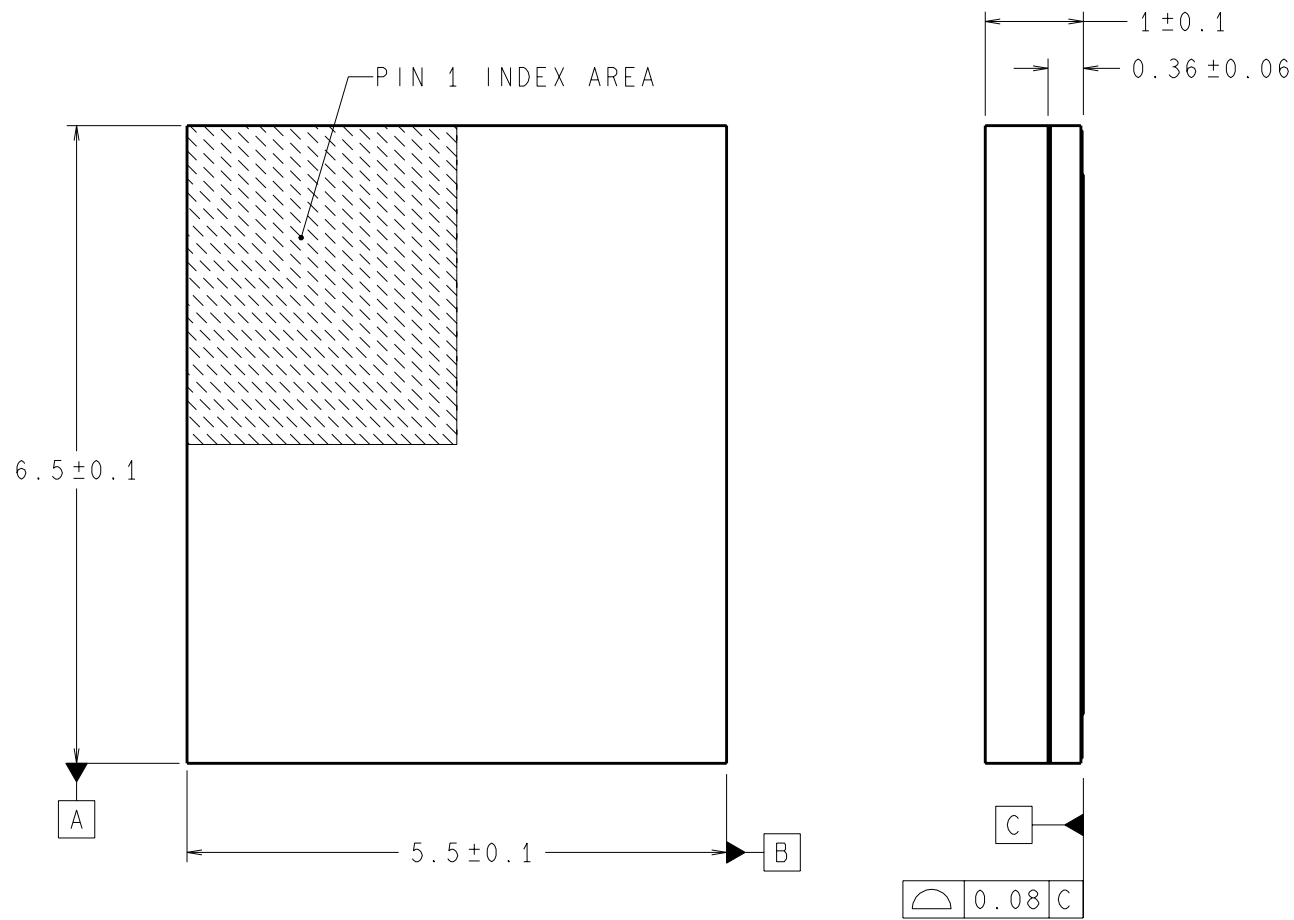


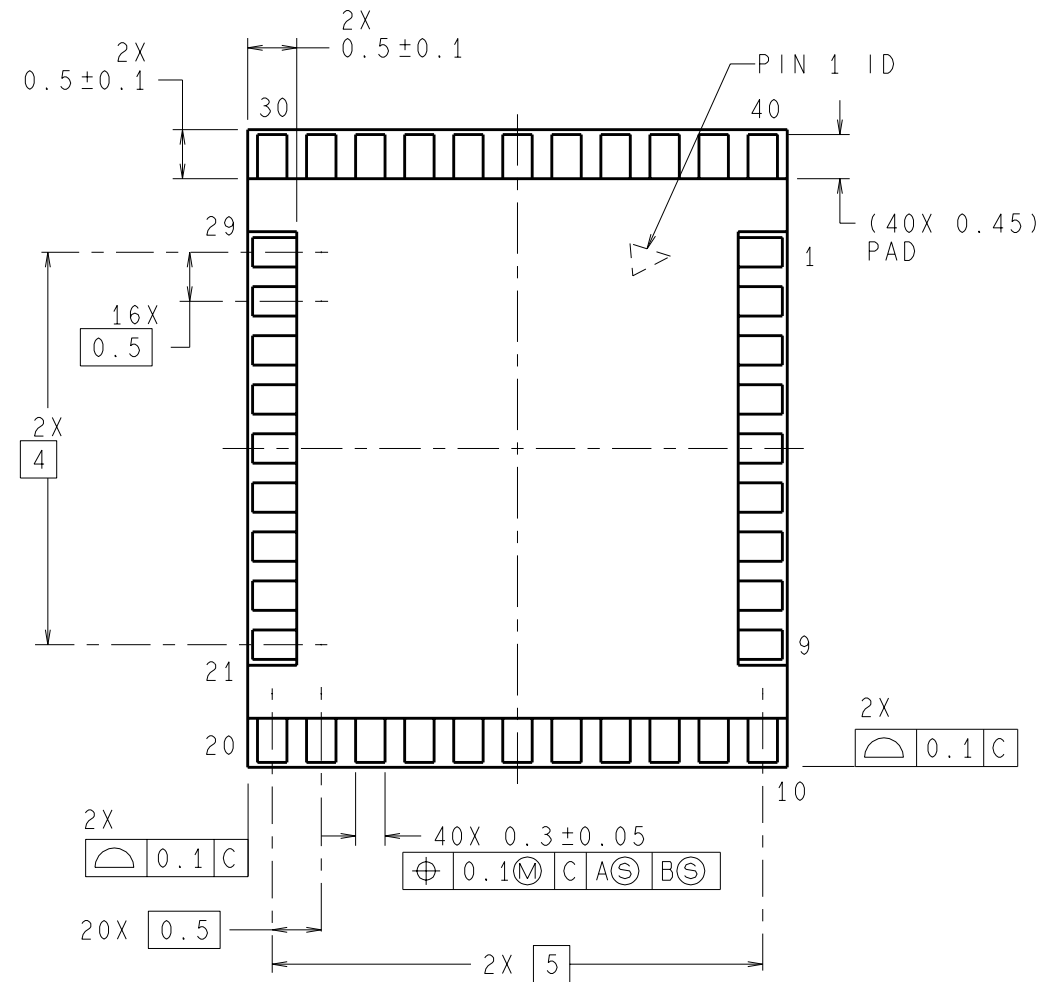
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	12453	05/11/2000	TL/WL



**RECOMMENDED LAND PATTERN**  
1:1 RATIO WITH PACKAGE SOLDER PADS



**DIMENSIONS ARE IN MILLIMETERS**



NOTES: UNLESS OTHERWISE SPECIFIED

- MATERIAL: BT RESIN CCL-HL832 WITH TAIYO PSR4000 AUS5 SOLDER MASK.
- PLATING: Cu 15 TO 20 MICROMETERS (FULL)  
Ni 10 ± 5 MICROMETERS (LEADS ONLY)  
Au 1 ± 0.5 MICROMETER (LEADS ONLY)
- REFERENCE JEDEC MO-208, VARIATION KFEA, DATED DECEMBER 1999.

APPROVALS		DATE	National Semiconductor	
DRAWN T. LEQUANG		05/11/2000	2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DFTG. CHK. MARTA SUCHY		05/11/2000	CSP, PLASTIC, LAMINATED, 6.5 X 5.5 X 1.0 mm BODY, 40 L, 0.5 mm PITCH, GENERIC	
ENGR. CHK. WAYNE LEE		05/11/2000		
		SCALE	SIZE	DRAWING NUMBER
		N/A	C	(SC)MKT-SLB40B
		DO NOT SCALE DRAWING		REV A
		SHEET 1 of 1		